

general purpose processor 18 references the selected storage element as memory mapped I/O via the internal address bus and either reads or writes to the selected storage element via the internal data bus.

Addition information regarding the present invention is provided in National Semiconductor Corporation's Advanced Data Sheet, NS32FX16, High Performance Fax Processor, which is provided as Appendix A at the end of this Detailed Description of the Invention.

It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention, that the structure and methods within the scope of these claims and their equivalence be covered thereby.

What is claimed is:

1. A data processing system for processing a digital signal, the data processing system comprising:
 - a shared bus for transferring both data and instructions;
 - a shared memory array for storing both data and general purpose instructions and that is connected for transfer of both data and general purpose instructions between the shared bus and the shared memory array;
 - a digital signal execution unit connected to the shared bus for processing the digital signal utilizing both data transferred between the shared memory array and the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred between the shared memory array and the digital signal execution unit on the shared bus; and
 - a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array
 whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor.
2. An integrated circuit data processing system for processing a digital signal, the data processing system comprising:
 - a shared internal bus for transferring both general purpose instructions and data;
 - a shared bus interface unit connected to the shared internal bus and connectable via a shared external bus to a shared external memory array via an external input/output port of the shared external memory array such that general purpose instructions and data stored in the shared external memory array may be transferred via external input/output port to be shared internal bus via the shared bus interface unit;
 - a digital signal execution unit connected to the shared internal bus for processing the digital signal utilizing both data transferred to the digital signal execution unit from the shared external memory array via the shared internal bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred to the digital signal execution unit from the shared external memory array via the shared internal bus; and
 - a general purpose processor connected to the shared internal bus for controlling the digital signal execution

unit by selecting each of the general purpose instructions to be transferred to the digital signal execution unit from shared external memory array via the shared internal bus

5 whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor.

3. An integrated circuit data processing system as in claim 10 2 and further comprising a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that general purpose instructions and data stored in the shared internal memory are transferrable via the internal input/output port of the shared internal memory array to the shared 15 internal bus for transfer to either the digital signal execution unit or the general purpose processor

whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is 20 selectively configurable by the general purpose processor selecting individual general purpose instructions from the shared external memory and/or the shared internal memory.

4. A data processing system for processing a digital signal. 25 the data processing system comprising:

a shared bus for transferring both data operands and general purpose instructions;

a shared memory array for storing both data operands and 30 general purpose instructions and that is connected for transfer of data operands and general purpose instructions between the shared bus and the shared memory array;

a digital signal execution unit connected to the shared bus 35 for processing the digital signal utilizing data operands transferred from the shared memory array to the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions 40 transferred from the shared memory array to the digital signal execution unit on the shared bus; and

a general purpose processor connected to the shared bus 45 for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array; and

wherein the digital signal execution unit includes

a control register connected to the shared bus for storing 50 a general purpose instruction transferred to the digital signal execution unit by the general purpose processor from the shared memory array on the shared bus;

a multiply/accumulate unit that responds to storage of said 55 general purpose instruction in the control register by initiating execution of a DSP operation corresponding to said general purpose instruction; and

a DSP address generator connected to the shared bus for 60 retrieving a first data operand stored in the shared memory and utilizable by the multiply/accumulate unit in executing said DSP operation.

5. A data processing system as in claim 4 wherein the multiply/accumulate unit includes first and second input 65 ports for receiving said first data operand and a second data operand respectively, for utilization by the multiply/accumulate unit in executing said DSP operation.

6. A data processing system as in claim 5 wherein the address generator includes means for retrieving both said

7. An integrated circuit data processing system for processing a digital signal, the data processing system comprising:

8. A data processing system as in claim 7 wherein the digital signal execution unit includes an internal address generator for retrieving operands from either the shared internal memory array or the external memory system via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions.
9. An integrated circuit data processing system for processing a digital signal, the data processing system comprising:

- (a) a digital signal execution unit that recovers digital data from the digital signal by executing a selected sequence of digital signal processor (DSP) instructions;
- (b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

5 (d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for
10 transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via
15 the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;
20 wherein the digital signal execution unit includes an internal address generator for retrieving operands from the shared internal memory array via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions.]

25 [10. An integrated circuit data processing system for processing a digital signal, the data processing system comprising:

(a) a digital signal execution unit that recovers digital data from the digital signal by executing a selected sequence of digital signal processor (DSP) instructions;

30 (b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

35 (c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected;

40 (d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for
45 transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via
50 the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;

55 wherein the DSP instructions and the general purpose instructions comprise subsets of a single instruction set executable by the data processing system; and

(e) an instruction sequencing unit connected to the shared internal bus for controlling the flow of execution of the DSP instructions and the general purpose instructions.]

11. A data processing system comprising:
a first bus;
a memory connected to the first bus;
a general purpose processor (GPP) connected to
the first bus, the GPP loading operands into the
memory; and
a digital signal processor (DSP) connected to
the first bus, the DSP having a register and starting
execution of an instruction in response to the GPP
loading information into the register.

12. The data processing system of claim 11
wherein the operands held in the memory are randomly
accessible.

13. The data processing system of claim 11
wherein the information placed in the register
identifies the instruction to be executed.

14. The data processing system of claim 11
wherein the DSP is connected to the memory via a
second bus.

15. The data processing system of claim 11 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

16. The data processing system of claim 11 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

17. The data processing system of claim 11 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

18. The data processing system of claim 11
wherein the DSP only executes a single instruction
when said information is loaded into the register.

19. The data processing system of claim 11
wherein the DSP retrieves the operands from the
memory.

20. A data processing system comprising:
a first bus;
a memory connected to the first bus;
a general purpose processor (GPP) connected to
the first bus, the GPP loading operands into the
memory; and

a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction.

21. The data processing system of claim 20
wherein the operands held in the memory are randomly
accessible.

22. The data processing system of claim 20 wherein the information placed in the register identifies the instruction to be executed.

23. The data processing system of claim 20 wherein the DSP is connected to the memory via a second bus.

24. The data processing system of claim 20 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

25. The data processing system of claim 20 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

26. The data processing system of claim 20 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

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27. The data processing system of claim 20 wherein the DSP only executes a single instruction when said information is loaded into the register.

28. The data processing system of claim 20 wherein the DSP retrieves the operands from the memory.

29. A data processing system comprising:
a first bus;
a memory connected to the first bus;
a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register.

30. The data processing system of claim 29 wherein the operands held in the memory are randomly accessible.

31. The data processing system of claim 29 wherein the information placed in the register identifies the instruction to be executed.

32. The data processing system of claim 29 wherein the DSP is connected to the memory via a second bus.

33. The data processing system of claim 29 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

34. The data processing system of claim 29 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

35. The data processing system of claim 29 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

36. The data processing system of claim 29 wherein the DSP only executes a single instruction when said information is loaded into the register.

37. A data processing system comprising:
a digital signal processor (DSP) that processes digital data by executing an algorithm that includes a specific sequence of DSP operations;

a general purpose processor (GPP) that selects the sequence of DSP operations for execution by the DSP from a basic set of DSP operations, and that performs general purpose tasks utilizing selected instructions and data;

a bus to which both the DSP and the GPP are connected;

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a memory connected to the bus such that the memory is accessible by the DSP for retrieving operands utilized by the DSP in executing the selected sequence of DSP operations and by the GPP for loading operands required for execution of the selected DSP algorithm and/or instructions and data for use by the GPP for controlling the DSP; and

a control register of the DSP characterized in that said GPP invokes a first DSP operation in the selected sequence by issuing a corresponding command directly to said control register of the DSP.

38. The system of claim 37 wherein the DSP, in response to receiving a first DSP operation, places the GPP in a continuous wait state while the DSP performs the first DSP operation utilizing operands retrieved from the memory.

39. The system of claim 37 wherein, upon completion of execution of the selected sequence of the DSP operations, the GPP downloads contents of the memory and retrieves a new set of operands, instructions, and data for a new sequence of DSP operations.

40. A data processing system comprising:
a first data bus;
a second data bus;
a memory connected to the first data bus and the
second data bus;
a general purpose processor (GPP) connected to
the first data bus, the GPP loading operands into the
memory via the first data bus; and
a digital signal processor (DSP) connected to
the first data bus and the second data bus, the DSP
executing an instruction identified by the GPP, and

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retrieving operands from the memory via the second
data bus.

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41. The data processing system of claim 40 wherein the operands held in the memory are randomly accessible.

42. The data processing system of claim 40 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

43. The data processing system of claim 40 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

44. The data processing system of claim 40 and further comprising:

a bus interface unit connected to the first data
bus; and

a third data bus connected to the bus interface
unit.

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